Fabrication and Characterization of Polymer-Enhanced TSVs, Inductors, and Antennas for Mixed-Signal Silicon Interposer Platforms

Paragkumar A. Thadesar, *Member, IEEE*, and Muhannad S. Bakir, *Senior Member, IEEE*

***Abstract*— This paper demonstrates the fabrication and high-frequency characterization of polymer-enhanced technologies for a mixed-signal silicon interposer platform. First, the fabrication of 60-μm-diameter and 285-μm-tall photodefined polymer-embedded vias is demonstrated. Their losses are extracted using L–2L and open–short de-embedding techniques up to 30 GHz followed by parasitics extraction. Moreover, eye-diagram measurements are demonstrated for the vias at 10 Gb/s. Second, the fabrication and impedance extraction of 65-μm-diameter and 285-μm-tall photodefined polymer-enhanced coaxial vias are demonstrated. Finally, utilizing the photodefined polymer-enhanced silicon interposer technology, high-performance inductor and antenna are demonstrated over polymer wells.**

***Index Terms*— Antennas, coaxial through-silicon vias (TSVs), de-embedding, eye diagrams, inductors, silicon interposer, TSV.**

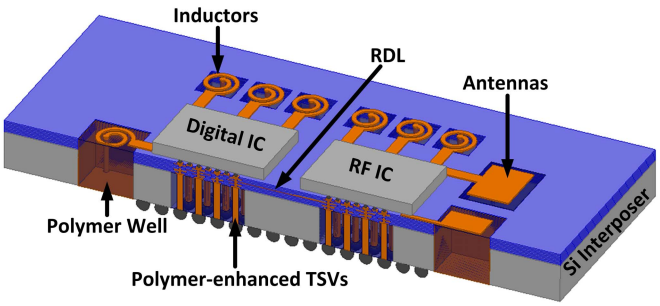

Fig. 1. Envisioned mixed-signal silicon interposer platform featuring polymer-enhanced TSVs, antennas, and inductors.

I. Introduction

SILICON interposers with dense fine-pitch metallization and through-silicon vias (TSVs) have widely been explored for high-bandwidth density communication between heterogeneous ICs [1]–[3]. Moreover, silicon interposers provide opportunities for the integration of inductors and antennas close to the ICs yielding compact radio-frequency (RF) and analog/mixed-signal systems. The integration of inductors on silicon interposers can improve the performance of circuits, such as digital-controlled oscillators, low-noise amplifiers, and power amplifiers [4]. Moreover, the integration of antennas on silicon interposers can enable a wide range of applications, specifically for those in the millimeter-wave frequency bands (30–300 GHz) with smaller antenna sizes. For example, the frequency band around 60 GHz has been explored for high-speed multimedia transfer and short-range communications [5]; the band around 28 GHz has been explored for future 5G communications [6]; the band around 77 GHz has been explored for radars in automobiles [7]; and the *D*-band has been explored for medical imaging and picocell cellular links [8].

For the integration of heterogeneous ICs with antennas and inductors close to the ICs, large-area silicon interposers are desired [5], [9]. Greater silicon thickness (larger than 300–400 μm) is desired as well for large-area interposers to minimize warpage and bow and improve mechanical stability [10], [11]. However, increasing the interposer thickness results in longer TSVs with increased losses [12]. These factors drive the need for low-loss TSV technologies for large-area thick interposers to compensate for the increased length. To reduce the TSV losses, thick polymer [13], air liners [14], and coaxial TSVs [15], [16] have been explored in the literature. In addition to the TSV loss, the presence of silicon near antennas and inductors results in lower radiation efficiency and *Q*-factor, respectively [17], [18]. This performance degradation demands innovative antenna and inductor integration technologies within silicon interposers. High-resistivity silicon and glass have been explored in the literature to obtain high-performance passives as well as low-loss TSVs [19], [20].

To address the need for novel low-loss TSVs and high-performance inductors and antennas on silicon interposers, this paper demonstrates the fabrication and characterization of a polymer-enhanced and photodefined silicon interposer platform featuring: 1) polymer-embedded via (PEV)

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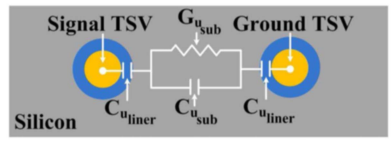
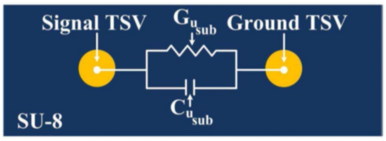


(a)



(b)

Fig. 2. Top view of parasitic schematic for signal–ground TSV pairs. (a) PEVs. (b) TSVs with SiO_2 liner.

fabrication, loss de-embedding up to 30 GHz, capacitance and conductance extraction, and eye-diagram measurements; 2) polymer-enhanced coaxial via fabrication and impedance extraction up to 50 GHz; 3) polymer-enhanced inductor fabrication, RF measurements, and Q and L extractions; and 4) polymer-enhanced antenna fabrication and W-band measurements. An envisioned mixed-signal system using the proposed technologies is shown in Fig. 1.

This paper describes the analysis, fabrication, and measurements of PEVs in Section II. The fabrication and characterization of polymer-enhanced coaxial vias are described in Section III. Finally, the fabrication and characterization of polymer-enhanced inductor and antenna are demonstrated in Section IV. Finally, the conclusion is drawn in Section V.

II. Polymer-Embedded Vias

Vias within dielectric regions in silicon have been shown in the literature, including: 1) metal-coated silicon pillars in polymer wells [21] and 2) copper vias in reflowed glass [22]. This paper focuses on utilizing SU-8 [23] photodefinition to fabricate low-loss PEVs.

A. Analysis

To compare the high-frequency parasitics of PEVs and TSVs with SiO_2 liner, an electrical analysis is performed for signal–ground TSV pairs. TSV high-frequency electrical modeling has widely been explored in [19] and [24]–[26]. TSVs, in this paper, are modeled using resistors and inductors with conductance and capacitances between the signal and ground TSVs, as shown in Fig. 2. For the TSVs with SiO_2 liner, the path between the signal and ground TSVs consists of per-unit-length substrate capacitance $C_{u_{\text{sub}}}$, substrate conductance $G_{u_{\text{sub}}}$, and dielectric capacitances $C_{u_{\text{liner}}}$. For PEVs, the path between the signal and ground TSVs consists of only per-unit-length substrate capacitance $C_{u_{\text{sub}}}$ and substrate conductance $G_{u_{\text{sub}}}$, since a dielectric liner is not present.

The formulas utilized for per-unit-length resistance, inductance, conductance, and capacitance ($RLGC$) evaluation are demonstrated in [19] and [25]. Once the per-unit-length

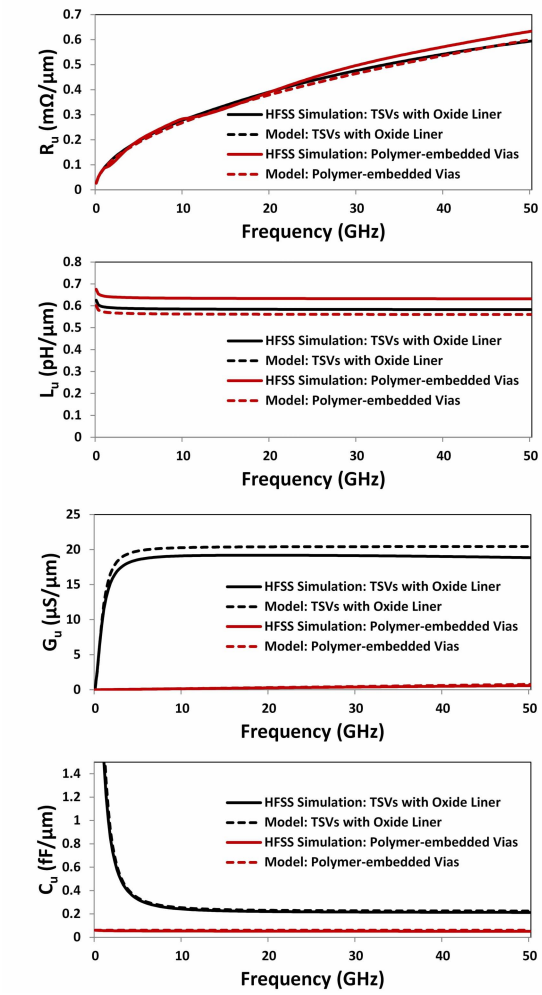


Fig. 3. Evaluated per-unit-length TSV $RLGC$ values using models and HFSS simulations.

$RLGC$ values are calculated, electromagnetic simulations are performed for comparison using ANSYS high-frequency structure simulator (HFSS), as described in [19]. The per-unit-length $RLGC$ values for the TSVs with SiO_2 liner and PEVs are shown in Fig. 3; copper vias are 70 μm in diameter and on a 150-μm pitch. The thickness of the SiO_2 liner is 1 μm. The relative dielectric constants of silicon and SiO_2 are 11.68 and 3.9, respectively [27]; silicon resistivity is 10 $\Omega \cdot$cm. Moreover, with respect to the properties of SU-8, broadband ϵ_r and tan δ characterizations have extensively been shown in the literature using techniques such as microstrip transmission lines, conductor-backed coplanar waveguide transmission lines, microstrip ring resonators, and T resonators [28]–[30]. The broadband ϵ_r and tan δ values characterized in the literature up to 210 GHz are close to 3 and 0.04, respectively, and have been used in this paper.

As shown in Fig. 3, PEVs attain 96.2% and 72.8% reduction in conductance and capacitance at 50 GHz, respectively, compared to TSVs with the SiO_2 liner and the same copper via dimensions. The reduction in the capacitance and conductance of PEVs provides a low-loss electrical performance and hence will be focused upon later in this paper.

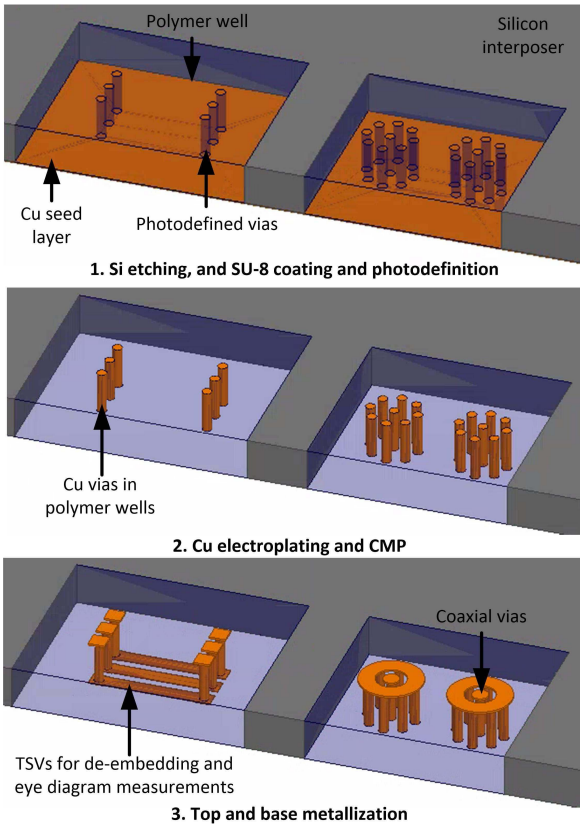


Fig. 4. Fabrication process for polymer-enhanced TSVs.

B. Fabrication

The fabrication process of the polymer-enhanced TSVs under consideration is shown in Fig. 4. The fabrication process begins with the formation of wells (using the Bosch process) in a silicon wafer containing a copper seed layer at the base. Next, SU-8 coating, photodefinition, via electroplating and chemical–mechanical polishing (CMP) are performed to obtain copper vias in the photodefined polymer wells [13]. The vias are fabricated in ground-signal-ground (GSG) and coaxial (described in Section III) configurations. Next, the top and base metallizations are fabricated over the copper vias to attain the following structures: 1) de-embedding and eye-diagram measurement structures with pads over the vias and traces at the base and 2) coaxial via impedance extraction structures, as described in Section III.

C. RF De-Embedding and CG Extraction

To perform de-embedding of PEVs, two methodologies are implemented: 1) L–2L [31] and 2) open–short [32]. The schematics of the structures fabricated and characterized for de-embedding are shown in Fig. 5(a). A standalone PEV structure is simulated for the sole purpose of benchmarking its results to those obtained from de-embedding. Moreover, a standalone TSV structure with SiO_2 liner is also simulated (for the comparison of PEVs to the TSVs with 1-μm-thick SiO_2 liner and 10-$\Omega\cdot$cm silicon resistivity). In the de-embedded TSV structures and the standalone structures for benchmarking, the contribution of the top and bottom pads

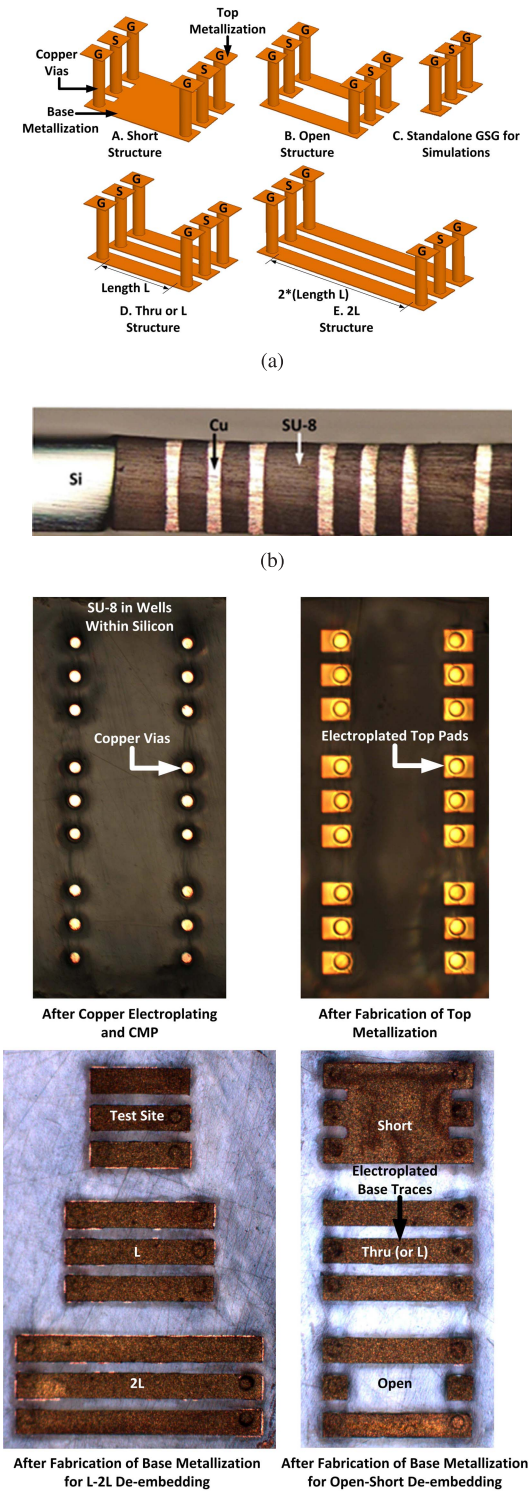


Fig. 5. PEVs. (a) Schematics of measured and simulated TSV structures for de-embedding. (b) Cross-sectional view of the fabricated vias. (c) De-embedding and time-domain (L or thru) measurement structures.

is included owing to the de-embedding methodologies used. With further development in de-embedding methodologies, a de-embedding of TSVs without pads can be obtained in the future.

Using the process in Fig. 4, the fabricated PEVs for de-embedding are shown in Fig. 5. The fabricated vias are

285-μm tall, 60 μm in diameter, and on a 150-μm pitch within 1800 μm $\times$ 1800-μm wells; the traces are 105-μm wide.

For L–2L de-embedding [31], TSV-trace-TSV structures with the 400- and 800-μm-long traces between the TSVs (with pads) were fabricated, simulated, and measured. The measured and simulated S-parameters of PEVs are converted to $ABCD$-parameters, and the TSV losses are extracted as follows:

$$\mathbf{ChainL} = \mathbf{TSV} * \mathbf{Trace} * \mathbf{TSV} \tag{1}$$

and

$$\mathbf{Chain2L} = \mathbf{TSV} * \mathbf{Trace} * \mathbf{Trace} * \mathbf{TSV} \tag{2}$$

where **ChainL**, **Chain2L**, **TSV**, and **Trace** represent the matrices of $ABCD$-parameters. Moreover, **ChainL** represents the TSV-trace-TSV structure with the 400-μm-long traces between the TSVs, **Chain2L** represents the TSV-trace-TSV structure with the 800-μm-long traces between the TSVs, **TSV** represents the GSG TSVs (with pads), and **Trace** represents the 400-μm-long GSG traces between the TSVs.

From (1) and (2)

$$\mathbf{TSV} = \sqrt{\mathbf{ChainL}^{-1} * \mathbf{Chain2L} * \mathbf{ChainL}^{-1}}^{-1}. \tag{3}$$

For open–short de-embedding [32], the TSV-trace-TSV structure with the 400-μm-long traces (thru or L structure), and open and short structures with the same distance between the TSVs were fabricated, simulated, and measured.

The open–short technique provides the losses of the traces at the base of the thru structure, which is followed by the extraction of the losses of GSG TSVs using $ABCD$ matrices. First, the S-parameters of the open, short, and thru structures are converted to Y-parameters to evaluate the following matrices:

$$\mathbf{Matrix1}_Y = \mathbf{Thru}_Y - \mathbf{Open}_Y \tag{4}$$

and

$$\mathbf{Matrix2}_Y = \mathbf{Short}_Y - \mathbf{Open}_Y. \tag{5}$$

Next, the evaluated Y-parameter matrices are converted to Z-parameter matrices, and the Z-parameters of the traces at the base of the thru structure are obtained as follows:

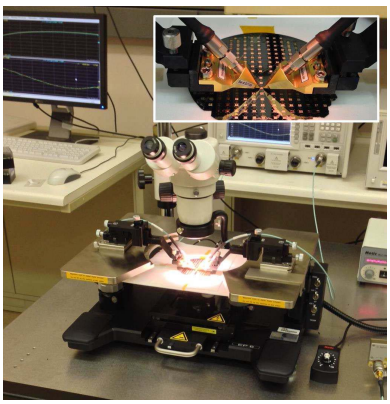
$$\mathbf{Trace}_Z = \mathbf{Matrix1}_Z - \mathbf{Matrix2}_Z. \tag{6}$$

Once the Z-parameters of the trace are obtained, they are converted to $ABCD$-parameters to extract the TSV losses from the thru structure as follows:

$$\mathbf{TSV} = \sqrt{\mathbf{Thru} * \mathbf{Trace}} * \mathbf{Trace}^{-1}. \tag{7}$$

To extract the TSV losses, RF measurements were performed up to 30 GHz using a probe station with a Keysight N5245A PNA-X network analyzer and Cascade MicroTech 150-μm pitch |Z| probes, as shown in Fig. 6(a). Prior to measurements, calibration was performed using the line-reflect-reflect-match protocol. The de-embedded TSV measurements are compared with HFSS simulations.

As shown in Fig. 6(b), the via losses attained from both de-embedding techniques are in good agreement up to 30 GHz with minor difference between the de-embedded and the standalone TSV loss. The de-embedding results from the measurements yield 0.22-dB insertion loss per PEV at 30 GHz. Compared with the simulated insertion loss of a standalone



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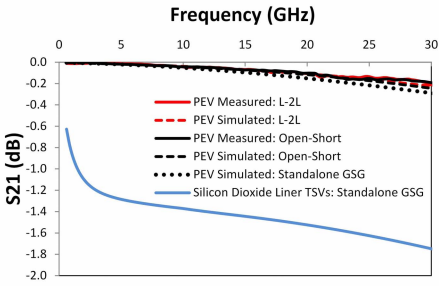

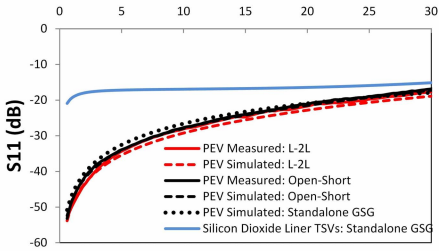

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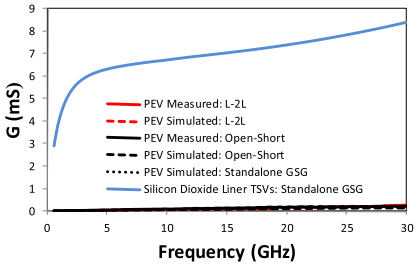

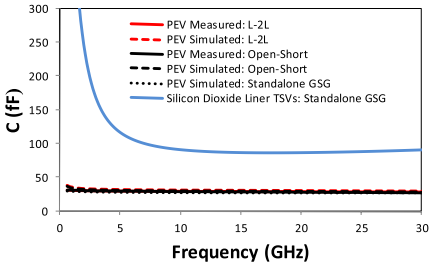

(c)

Fig. 6. (a) PEV RF measurement setup. (b) De-embedded results. (c) CG extractions.

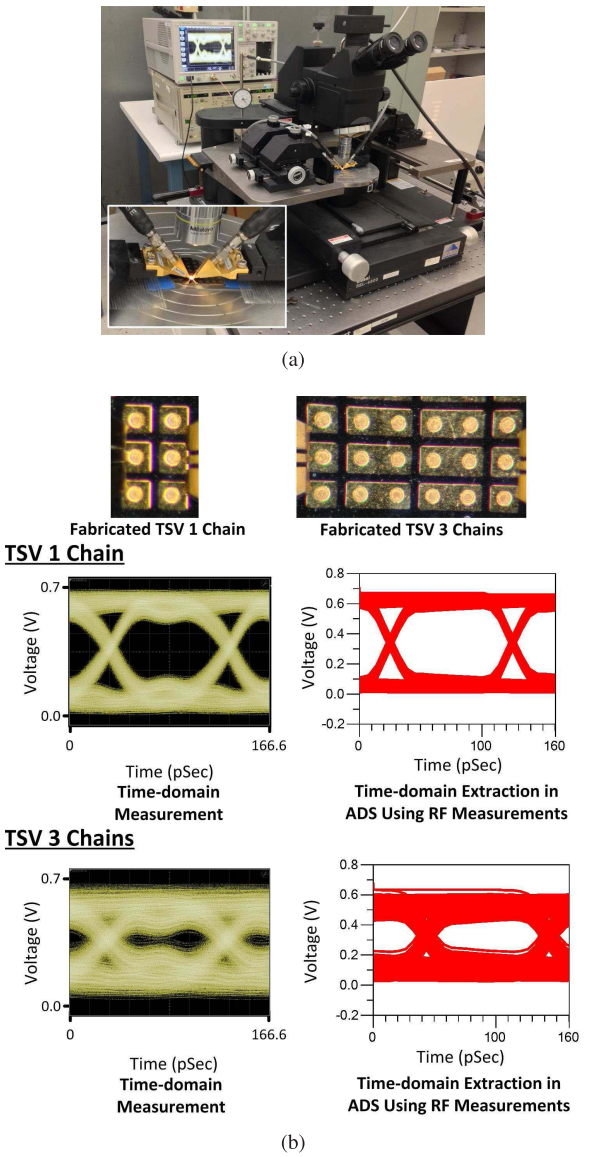

Fig. 7. TSV time-domain measurement. (a) Measurement setup. (b) Time-domain measurements and extractions in ADS using RF measurements of the TSVs with SiO_2 liner.

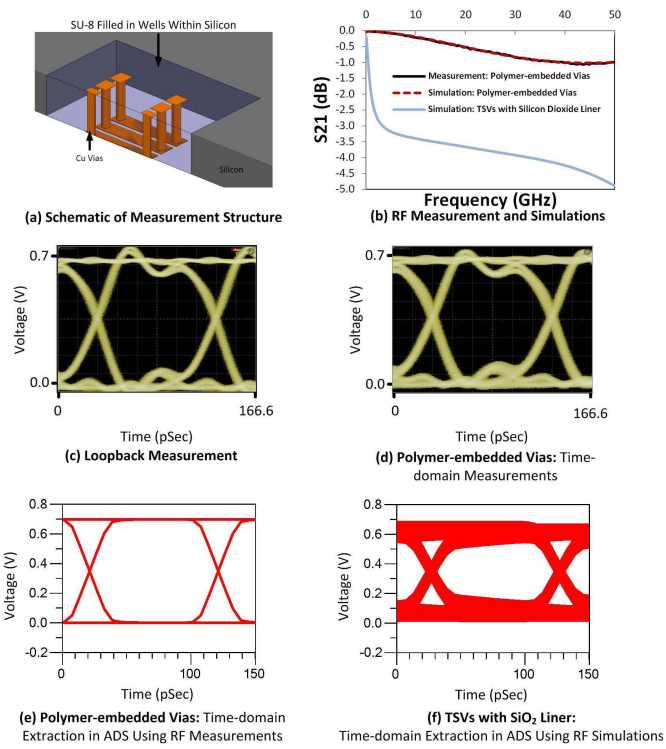

Fig. 8. Measured eye diagrams of PEVs with constructed eye diagrams in ADS using the RF measurements of PEV chains. Loop-back measurement and extracted eye diagrams from the RF simulations of the TSVs with SiO_2 liner are also shown for benchmarking.

TSV with SiO_2 liner, 87% reduction in insertion loss can be obtained using the PEVs at 30 GHz.

Moreover, since the key contribution to the low-loss behavior of PEVs results from the reduced capacitance and conductance compared with the TSVs with SiO_2 liner (Fig. 3), capacitance and conductance of the de-embedded GSG PEVs are extracted using Y-parameters (obtained from the measured and simulated S-parameters) [25], [26]. The C and G extractions demonstrate a significant reduction in the capacitance and conductance for PEVs, as shown in Fig. 6(c).

D. Eye-Diagram Characterization

Eye diagrams assess intersymbol interference, jitter, and skew, and can thereby provide insight into TSV link performance. For TSV eye-diagram measurements, a setup, including an Anritsu MP1761C pulse pattern generator and an Agilent DCA-X 86100D oscilloscope, was used with Cascade MicroTech 150-μm and 200-μm pitch |Z| probes, as shown in Fig. 7(a). The measurements were performed with a 0.7 V (limited by the oscilloscope measurement capability) pseudo-random bit sequence (PRBS) of $2^{11}-1$.

To perform the eye-diagram characterization of the fabricated PEVs, first, the measurements of chains of TSVs with SiO_2 liner were performed; the TSVs are 88 μm in diameter, 300-μm tall, and formed on a 250-μm pitch with the 1-μm-thick SiO_2 liner. The measured eye diagrams at 10 Gb/s for one and three chains of TSVs are shown in Fig. 7(b).

To better understand the eye-diagram measurements, S-parameter measurements of the TSV chains are performed first [using the setup in Fig. 6(a)] and imported in Keysight's Advanced Design System (ADS) to obtain eye-diagram extractions using a transient analysis. For the transient analysis, a PRBS voltage source (VtPRBS) is applied at the input (with an internal 50-Ω impedance in series corresponding to a pattern generator), and a 50-Ω termination impedance is used at the output (corresponding to an oscilloscope) of the TSV chains. With the source and termination 50-Ω impedances, the VtPRBS generates a 0.7 V peak-to-peak PRBS of $2^{11}-1$ with a rise-and-fall time of 30 ps [33]. The extracted eye diagrams in ADS exhibit trends and eye openings similar to the time-domain measurements. The measurements show an additional loss from cables and probes compared with the extraction yielding smaller eye openings.

Next, the eye-diagram measurements of the fabricated PEVs [the L or Thru structure in Fig. 5(a)] are explored. Before

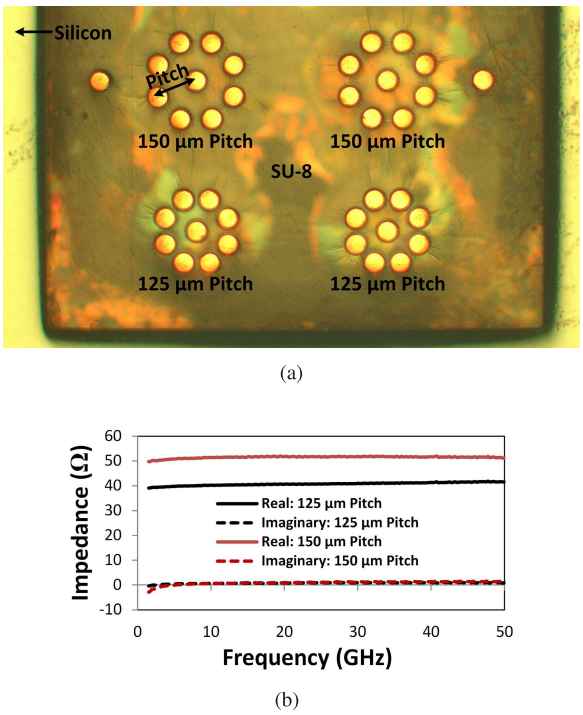

Fig. 9. Polymer-enhanced coaxial vias. (a) Top view of the fabricated vias. (b) Extracted impedance from TSV measurements.

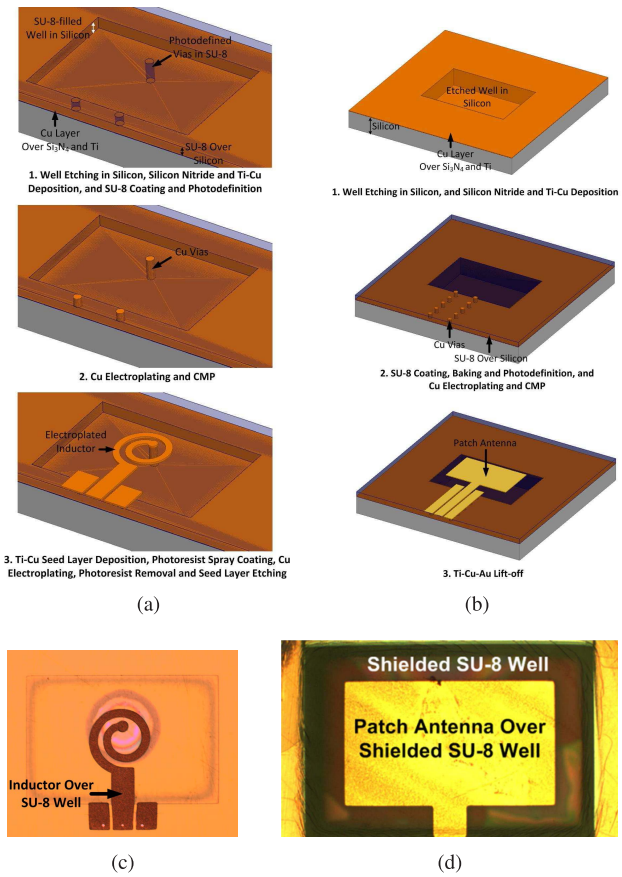

Fig. 10. Fabrication processes of (a) polymer-enhanced inductors and (b) polymer-enhanced antennas. Fabrication results of (c) inductor and (d) antenna.

performing the eye-diagram measurements, loop-back measurements with a direct connection of the pattern generator to the oscilloscope were performed. Next, similar eye-diagram measurements are performed (for the fabricated PEVs) to the TSVs with SiO_2 liner, as shown in Fig. 8. Moreover, using the eye-diagram extraction methodology in Keysight's ADS, eye diagrams are generated from the RF measurements of the fabricated PEVs and from the HFSS simulations of the TSVs with 1-μm-thick SiO_2 liner (10-$\Omega\cdot$cm silicon resistivity) and the same copper via dimensions. The PEV measurements demonstrate a minimal eye closing compared with the loop-back measurements and improved eye openings and timing jitters compared with the TSVs with SiO_2 liner.

III. Polymer-Enhanced Coaxial Vias

Various coaxial TSV techniques have been shown in the literature, including laser-ablated dielectric based coaxial TSVs with annular and cylindrical signal conductors and photodefined coaxial TSVs fabricated using a temporary release layer [15], [16], [34]. This paper demonstrates coaxial vias by extending the previously described process for PEVs.

The fabrication process of coaxial vias is shown in Fig. 4. Fig. 9(a) shows the fabricated 285-μm-tall polymer-enhanced coaxial vias within an 1800-μm $\times$ 1800-μm well in a silicon wafer (prior to the top layer metallization). The copper via diameter is 65 μm, and the signal-to-ground via pitches are 150 and 125 μm (i.e., two different coaxial vias).

The coaxial structure with the top metallization (Fig. 4) yields an electrically open structure for single-port measurements. Fabricating a copper layer at the base of the open structure yields an electrically short structure for single-port measurements. Using the open and short structures, high-frequency single-port measurements are performed from 1 GHz to 50 GHz. Using the measured S-parameters of the fabricated coaxial vias, Z-parameters and Y-parameters are obtained with 50 Ω as the reference impedance. Using the Z-parameters of the short structure, R and L are extracted, using the Y-parameters of the open structure, C and G are extracted [25]. Using the extracted $RLGC$, impedance is evaluated, as shown in Fig. 9(b), demonstrating a wide-band impedance matching to approximately 50 Ω using the 150-μm pitch vias and approximately 40 Ω using the 125-μm pitch vias.

IV. Polymer-Enhanced Inductor and Antenna

With respect to the RF inductors, various techniques have been demonstrated in the literature, including off-chip inductors that are: 1) formed over dielectric-coated trenched silicon [18]; 2) over glass interposers [9]; 3) using vias in the glass interposers [9]; 4) under a molding compound [4]; and 5) over polymer wells [35]. The inductor in this paper is implemented utilizing the photodefined polymer-enhanced silicon interposer technology demonstrated earlier yielding a high Q-factor using a one-port measurement structure. The proposed inductor can be fabricated in parallel to PEVs, easing the fabrication of the envisioned silicon interposer system, as shown in Fig. 1. The inductors are fabricated over shallow

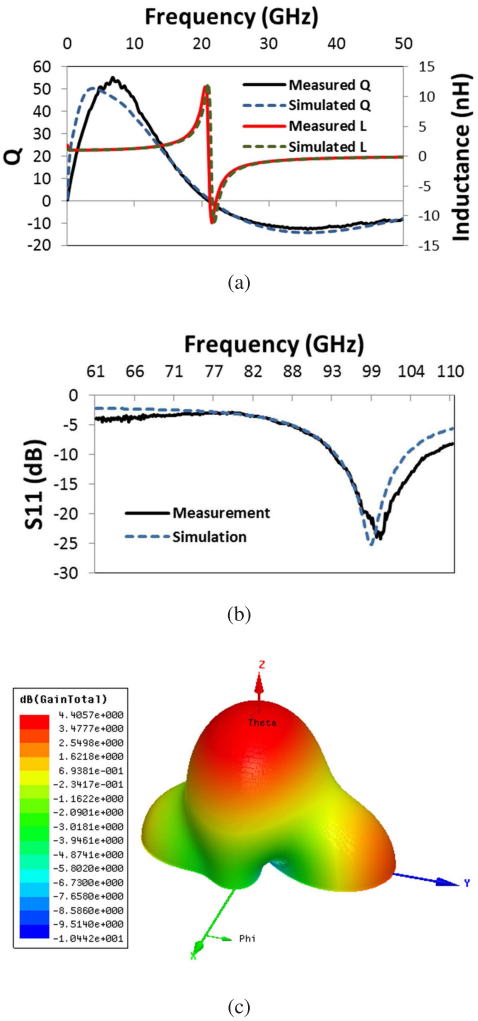

Fig. 11. Measurement results of (a) inductor, (b) antenna, and (c) antenna gain simulation.

wells (100-μm deep) in a silicon wafer to ease fabrication, and since an appreciable improvement is not observed in the Q-factor beyond 100-μm well depth. Spiral inductors have been implemented with the photodefined copper vias in the polymer wells to show the benefits of the photodefined polymer-enhanced silicon interposer technology using a simpler inductor geometry.

With respect to the antennas, various techniques have been demonstrated in the literature, including antennas over: 1) high-resistivity silicon with cavity backing [5]; 2) molding material [36]; 3) suspended SU-8 substrate [37]; and 4) polymer-filled wells [38]. Similar to the inductor, utilizing the photodefined polymer-enhanced silicon interposer technology, a high radiation-efficiency antenna is demonstrated in this paper. Various microfabricated antenna types, such as patch, folded dipole, slot, and Yagi-Uda, have been explored in [5] and [38]–[40]. Patch antennas have been selected in this paper owing to their ease of fabrication and good radiation control [41]. The rectangular patch has been selected instead of circular, elliptical, triangular, or annular shapes in order to achieve higher gain and bandwidth [41].

A. Fabrication

As shown in Fig. 10, the fabrication processes of the inductor and antenna begin with the etching of wells in a silicon wafer followed by silicon nitride and titanium-copper deposition. Next, SU-8 filling, photodefinition, copper electroplating, and CMP are performed followed by the fabrication of the inductors and antennas. The inductors are fabricated using electroplating, and antennas are fabricated using lift-off.

Fig. 10(c) shows the fabricated 8–12-μm-thick 1.5 turn inductor with the 55–65-μm-wide traces on a 100-μm pitch, and over a 1530 μm $\times$ 1030 μm and 100-μm deep well. Moreover, Fig. 10(d) shows the fabricated 1100 μm $\times$ 650 μm and 2-μm-thick patch antenna over a 1530 μm $\times$ 1030 μm and 280-μm deep well.

B. Characterization

For the fabricated inductor, high-frequency measurements were performed up to 50 GHz, and inductance and Q-factor were extracted demonstrating a peak Q-factor of 55 at 6.75 GHz ($f_{Q_{\text{peak}}}$) and a 1.14-nH inductance at $f_{Q_{\text{peak}}}$ with a self-resonance frequency at 21 GHz, as shown in Fig. 11(a).

Moreover, for the fabricated antenna, high-frequency measurements were performed from 60 GHz to 110 GHz demonstrating a 13.35-GHz 10-dB return loss bandwidth at the center frequency of 100 GHz, as shown in Fig. 11(b). In addition, an HFSS simulation of the fabricated antenna shows a gain of 4.4 dBi and 70% radiation efficiency at 100 GHz. A radiation pattern simulation result is shown in Fig. 11(c) demonstrating a high-gain primary lobe. A further improvement in the gain, radiation efficiency, and radiation pattern could be obtained by improving the antenna and feed designs, and using a polymer material with a lower loss tangent (benzocyclobutene, for example) in the future.

V. Conclusion

This paper demonstrates the fabrication and characterization of photodefined PEVs, coaxial TSVs, inductors, and antennas for mixed-signal heterogeneous integration using silicon interposers. RF analysis, fabrication, de-embedding up to 30 GHz, and eye-diagram measurements are demonstrated for PEVs, showing their enhanced electrical performance compared with the TSVs with SiO_2 liner. Moreover, fabrication and impedance extraction are demonstrated for coaxial TSVs showing wideband impedance matching. Finally, the fabrication and characterization of polymer-enhanced inductor and antenna are demonstrated proving their enhanced electrical performance.

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